Computer architecture

Homework week 13

Instructions

Submit by e-mail to the lecturer, as a PDF document with your name and student ID near the beginning. You can work in groups of 2, however, use different groups than week 10 and 11. Use the English language. Deadline: Dec 2nd, 23:59.

Question 1 (3pt)

1) Explain the types of hazards encountered in an in-order scalar processor.
2) Explain what additional hazards are encountered in superscalar processors, with example programs that trigger these hazards.
3) Outline the techniques that can be used to mitigate the hazards from #1.
3) Outline the techniques that can be used to mitigate the hazards from #2.

Question 2 (4pt)

1) Using the Intel Pentium 4 and Transmeta's Crusoe processors as examples, research and explain what *micro-code* and *trace caches* are in your own words.

   Be careful to use multiple infromation sources, since the most prominent seem to be largely incomplete.
2) Make a small diagram that shows where micro-code is translated and where a trace cache can be placed.

Question 3 (3pt)

A 22-stage pipeline with a branch predictor and only one execution path resolves branch instructions at the 8th stage. A given program which executes on average one branch per 40 instructions, causes a 82% misprediction rate in this pipeline.

Estimate the closest theoretical maximum for the average number of instructions per cycle of this program.

> **Note**
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> Obviously this pipeline has at most 1 IPC, but based on the information provided you can set a lower upper bound than 1 on the average IPC.